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APPLICATION FOR LETTERS PATENT

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Semiconductor Processing Methods Of Forming Dynamic Random Access Memory (DRAM) Circuitry

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SEMICONDUCTOR PROCESSING METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY (DRAM) CIRCUITRY

TECHNICAL FIELD

This application relates to semiconductor processing methods of forming dynamic random access memory (DRAM) circuitry.

BACKGROUND OF THE INVENTION

Dynamic random access memory (DRAM) circuitry is typically formed by forming a number of different layers of material over a substrate such as a silicon wafer, and then etching such layers into desired substrate features such as conductive word lines, capacitor containers, capacitor structures, and bit lines to name just a few. Efforts continue to be made to reduce the number of processing steps and processing complexity thereof.

This invention arose out of concerns associated with improving the methods through which dynamic random access memory (DRAM) circuitry is formed. This invention also arose out of concerns associated with reducing processing complexities associated with the fabrication of DRAM circuitry.

SUMMARY OF THE INVENTION

Methods of forming dynamic random access memories (DRAM) are described. In one embodiment, an insulative layer is formed over a substrate having a plurality of conductive lines which extend within a

memory array area and a peripheral area outward of the memory array. Capacitor container openings and contact openings are contemporaneously etched over the memory array and conductive line portions within the peripheral area respectively.

In another embodiment, a patterned masking layer is formed over a substrate having a plurality of openings formed within an insulative layer, wherein some of the openings comprise capacitor container openings within a memory array and other of the openings comprise conductive line contact openings disposed over conductive lines within a peripheral area outward of the memory array. With a common patterned masking layer, unmasked portions of a capacitor electrode layer are removed within the memory array and material from over portions of the conductive lines within the peripheral area is removed sufficient to expose conductive material of the conductive line portions.

In yet another embodiment, a common etch chemistry is used to remove selected material of an insulative material layer formed over conductive lines within a peripheral area and material of a storage capacitor electrode layer.

In yet another embodiment, a plurality of conductive plugs are formed over substrate node locations over which storage capacitors are to be formed. After forming the plugs, insulative material over conductive lines within a peripheral area is removed to first expose conductive material of the conductive lines.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 7.

Fig. 9 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 8.

Fig. 10 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 9.

Fig. 11 is a diagrammatic side sectional view of a semiconductor wafer fragment in process in accordance with another embodiment of the invention.

Fig. 12 is a view of the Fig. 11 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 11.

Fig. 13 is a view of the Fig. 11 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 12.

Fig. 14 is a view of the Fig. 11 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 13.

Fig. 15 is a view of the Fig. 11 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 14.

Fig. 16 is a view of the Fig. 11 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment in process is shown generally at 20 and includes a semiconductive substrate 22. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other

materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A plurality of conductive lines 24, 26, 28, and 30 are formed over substrate 22. Conductive lines 26, 28, and 30 are formed over or within a memory array area 32, and conductive line 24 is formed over or within a peripheral area 34 outward of memory array area 32. An isolation oxide region 36 is provided within substrate 22, as are diffusion regions 38, 40 which constitute node locations with which electrical communication is desired. The conductive lines typically include a gate oxide layer 42, an overlying polysilicon layer 44, a silicide layer 46, and an insulative material layer or cap 48. For purposes of the ongoing discussion, insulative material layer 48 comprises a first insulative material layer. Exemplary materials for insulative caps 48 include nitrogen-containing material and, in a preferred embodiment, silicon-containing material such as silicon nitride. Sidewall spacers 50 are provided over conductive lines 24-30. Of course, other conductive line constructions can be utilized.

Referring to Fig. 2, a conductive material layer 52 is formed over substrate 22. An exemplary material is conductively doped polysilicon.

Referring to Fig. 3, a plurality of conductive plugs, such as exemplary conductive plug 54, are formed and received over substrate node locations over which storage capacitors are to be formed.

Referring to Fig. 4, an insulative layer 56 is formed over substrate 22 and conductive lines 24-30. For purposes of the ongoing discussion, layer 56 constitutes a second insulative material. An exemplary material is borophosphosilicate glass (BPSG).

Referring to Fig. 5, a plurality of openings 58, 60 are formed and received within insulative layer 56. Opening 58 comprises a contact opening which is formed over insulative cap 48 of conductive line 24, and opening 60 comprises a capacitor container opening within which a storage capacitor is to be formed.

In one embodiment, openings 58, 60 are contemporaneously etched within the memory array area and within the peripheral area. Such openings preferably have substantially the same opening dimensions. Preferably, the openings are etched to expose the insulative caps of one or more of the conductive lines. In this example, the openings within the peripheral area, as initially formed, expose first insulative material cap 48 therewithin, but not conductive material of the conductive lines. Preferably, opening 60 exposes portions of conductive plug 54 within the memory array. For purposes of the ongoing discussion, opening 58 constitutes a first contact opening which is formed over insulative cap 48 within the peripheral area.

Referring to Fig. 6, a conductive material 62 is formed over the substrate and within the openings. In the illustrated example, material 62 comprises a first capacitor electrode layer in the form of a storage node layer which is formed within openings 58, 60.

Exemplary materials for layer 62 include conductively doped silicon-containing materials such as polysilicon, hemispherical grain polysilicon or cylindrical grain polysilicon. In this example, hemispherical grain polysilicon is shown. After formation of conductive material 62, selected portions can be removed, as by planarization, to isolate the material within the openings. A dielectric layer 64 is formed over the substrate and within openings 58, 60, and a conductive material 66 is formed over the substrate and within the openings. In the illustrated example, material 66 comprises an outer or second capacitor electrode layer in the form of a cell plate layer which is formed over dielectric layer 64. Collectively, layers 62, 66 constitute a pair of capacitor electrode layers which are formed within openings 58 and 60 and separated by an intervening dielectric region therebetween. A patterned masking layer 68 is formed over substrate 22 and within capacitor container opening 60. An exemplary material is photoresist.

Referring to Fig. 7, selected unmasked conductive cell plate material of cell plate layer 66 within memory array area 32 is patterned away or otherwise removed, and conductive material from within contact opening 58 (i.e. layer 62) is removed from over a portion of conductive line 24.

Referring to Fig. 8, and with common patterned masking layer 68 in place, remaining unmasked portions of the capacitor electrode layer(s) within the peripheral area are removed as well as insulative material 48 from over conductive line 24. The removal of the insulative material

preferably exposes conductive material of conductive line 24, e.g. silicide material 46 and constitutes removing insulative cap portions from over the conductive line portions. Although not specifically shown, the height of layer 56 can be reduced during the removal of the unmasked portions of the capacitor electrode layer(s) within the peripheral area and the insulative material 48 from over conductive line 24.

In a preferred embodiment, the removal of insulative material 48 and conductive material of the capacitor electrode layers is conducted using a common etch chemistry. For example, where insulative material 48 comprises silicon nitride and the capacitor electrode layers comprise polysilicon, an etch chemistry including NF_3 and HBr can be utilized to etch silicon-containing and silicon nitride-containing materials selective to oxides such as BPSG. Accordingly, conductive material is removed from within the memory array contemporaneously with conductive material which is removed from within contact openings 58 within the peripheral area. Hence, capacitor electrode material is removed from within contact openings 58 and not from within capacitor container openings 60.

In a preferred embodiment, the removal of insulative material portions 48 from over conductive line 24 constitutes a first-in-time exposure of conductive material of the conductive line in the peripheral area after provision of the insulative material thereover. Alternately considered, substantial portions of individual conductive line insulative caps are removed from the conductive lines which are formed over or

within peripheral areas 34. Preferably, the insulative material is removed using an etch chemistry which is also effective to remove both conductive material portions over the first insulative material and the first insulative material.

Referring to Fig. 9, an insulative layer 70 is formed over substrate 22. An exemplary material is BPSG.

Referring to Fig. 10, a contact opening 72 is formed within layer 70 and exposes portions of conductive material 46. Openings 73 within the memory array can also be formed and conductive material 74 formed therein to provide bit line contact plugs. Accordingly, such constitutes, with respect to conductive line 24, forming additional conductive material over and in electrical communication with the conductive line portions which were previously exposed.

Referring to Fig. 11, a semiconductor wafer fragment in process is shown generally at 20a. Like numerals from the above described embodiment have been utilized where appropriate with differences being indicated with the suffix "a" or with different numerals. A conductive material layer 52 is formed over substrate 22.

Referring to Fig. 12, a conductive plug 54 is formed over diffusion region 38, and conductive material 76 is formed or received over portions of some of the conductive lines within peripheral area 34. Accordingly, conductive material is formed over insulative material 48 of conductive line 24.

Referring to Fig. 13, an insulative layer 56 is formed over substrate 22 and subsequently openings 58, 60 are etched therethrough. In the illustrated example, openings 58, 60 expose portions of conductive plug 54 and conductive material 76.

Referring to Fig. 14, capacitor electrode layer 64 is formed over the substrate and within openings 58, 60, a dielectric layer 64 is formed thereover, and an outer or second capacitor electrode layer 66 is formed over the dielectric layer. Patterned masking layer 68 is formed over the substrate.

Referring to Figs. 15 and 16, unmasked portions of the storage capacitor electrode layers within the memory array and peripheral area are removed sufficiently to form a storage capacitor within the memory array, and to entirely remove the storage capacitor electrode layer from within the peripheral area. Preferably, such removal also outwardly exposes conductive portions of conductive line 24 within a peripheral area. Processing can now take place substantially as described above with respect to Figs. 9 and 10.

Advantages achieved with the present methods can include reductions in the processing steps required to form memory circuitry, as well as reductions in concerns associated with under- and over-etching substrate portions during fabrication. Other advantages will be apparent to the skilled artisan.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical

features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.